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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1) ☒ Responsive to communication(s) filed on *27 May 2009*.
2a) ☐ This action is **FINAL**.     2b) ☒ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4) ☒ Claim(s) *1-6 and 11* is/are pending in the application.
    4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) *1-6, and 11* is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9) ☐ The specification is objected to by the Examiner.
10) ☒ The drawing(s) filed on *19 June 2006* is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
    a) ☐ All   b) ☐ Some * c) ☐ None of:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____.
      3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
    * See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

### *Response to Arguments*

1.      Applicant's arguments with respect to claims 1-11 have been considered but are

moot in view of the new ground(s) of rejection.

Accordingly, claims 1-5, and 11, are pending, and claims 6-10, are cancelled.

### *Drawings*

The drawings are objected to because a label describing reference characters 5,

and 21-30, should be included in Figs. 4-6 and Fig. 8. For example, the label "multi-

stage binary search block" could be used to describe reference character 21 in Fig. 5.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in

reply to the Office action to avoid abandonment of the application. Any amended

replacement drawing sheet should include all of the figures appearing on the immediate

prior version of the sheet, even if only one figure is being amended. The figure or figure

number of an amended drawing should not be labeled as "amended." If a drawing figure

is to be canceled, the appropriate figure must be removed from the replacement sheet,

and where necessary, the remaining figures must be renumbered and appropriate

changes made to the brief description of the several views of the drawings for

consistency. Additional replacement sheets may be necessary to show the renumbering

of the remaining figures. Each drawing sheet submitted after the filing date of an

application must be labeled in the top margin as either "Replacement Sheet" or "New

Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner,

the applicant will be notified and informed of any required corrective action in the next

Office action. The objection to the drawings will not be held in abeyance.

## *Claim Rejections - 35 USC § 112*

1.      The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly
> claiming the subject matter which the applicant regards as his invention.

Claim 1, rejected under 35 U.S.C. 112, second paragraph, as being indefinite for

failing to particularly point out and distinctly claim the subject matter which applicant

regards as the invention.

As per claim 1, variable "W" is not clearly defined in the claim.  As such it is

unclear from the claim language.

Applicant is advised to carefully review claim 1, for compliance with 35 U.S.C.

112 2$^{nd}$ Paragraph.

The following art rejection is applied to applicant claims as best understood in

view of the 112 2$^{nd}$ paragraph rejections above.

## *Claim Rejections - 35 USC § 103*

1.      The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

2.      Claim 1, rejected under 35 U.S.C. 103(a) as being unpatentable over Toshihiko

(EP 0104449 A2).


As per claim 1, Toshihiko discloses a device for determining k representative of

the magnitude A of an orthogonal component of a Quadrature Amplitude Modulation

(QAM) symbol, including:

multi-stage binary search circuitry (Toshihiko, Fig. 1,34:42, $1^{st}$ and $2^{nd}$ detector,

which perform multi-stage binary search) for conducting a multi-stage binary search

(Toshihiko, Fig. 1,34:42, $1^{st}$ and $2^{nd}$ detector, which perform multi-stage binary search)

for the value of A (Toshihiko, Fig. 2A, Page 9, lines, 17-18, rectifying level) between

predetermined maximum and minimum values Amax (Toshihiko, Fig. 2A,high rectify

level, which is in this case maximum amplitude) and Amin (Toshihiko, Fig. 2A,low rectify

level, which is in this case minimum amplitude), each stage producing a single bit binary

output (Toshihiko, page 19, lines 24-27); and

integer value construction circuitry (Toshihiko, Fig. 1) for constructing the integer

value k (Toshihiko, page 3, lines 11-21) by juxtaposing the binary outputs (Toshihiko,

Fig. 1:60, adder) from consecutive stages of the binary search (Toshihiko, Fig. 1, which

shows consecutive stages of binary search),

n equals 2i and i is an integer (Toshihiko, page 3, lines 17-18),

Amax is a maximum detectable level of the magnitude A (Toshihiko, Fig. 2A, high

rectify level, which is in this case maximum amplitude),

Amin is a minimum detectable level of the magnitude A (Toshihiko, Fig. 2A, low

rectify level, which is in this case minimum amplitude), and

W is the incremental level (Toshihiko, page 10, lines 4-6, in this case AL1

represents W) between consecutive values of the integer value k (Toshihiko, page 3,

lines 11-21).

Even though Toshihiko does not specifically discloses W=(Amax-Amin)/n.

Toshihiko does disclose Amax, Amin, n and W.

At the time of the invention, it would have been obvious to one ordinary skill in

the art to subtract minimum amplitude from maximum amplitude and divide by

variable "n" to achieve the value of W.

The motivation would be to provide a demodulator which is capable of carrying

out both the phase control and gain control operations, as taught by Toshihiko.

(Toshihiko, page 3, lines 2-4)


3.      Claims 2-4, rejected under 35 U.S.C. 103(a) as being unpatentable over

Toshihiko (EPO 0104449 A2), and further in view of Brooks (US patent# 6185593 B1).


As per claim 2, Toshihiko further discloses a device according to claim 1, wherein

each orthogonal component sample (Toshihiko, page 3, lines 7-12) and the

predetermined maximum value Amax (Toshihiko, Fig. 2A, high rectify level, which is in

this case maximum amplitude) are in a floating point format comprising a mantissa

(Toshihiko page 3, lines 12-19) and an exponent (Toshihiko page 3, lines 12-19), and

wherein the multi-stage binary circuitry (Toshihiko, Fig. 1,34:42, 1<sup>st</sup> and 2<sup>nd</sup> detector,

which perform multi-stage binary search) to the exponent of the predetermined

maximum value Amax (Toshihiko, Fig. 2A, high rectify level, which is in this case

maximum amplitude).

Toshihiko does not disclose exponent normalizing circuitry for bit-shifting the

mantissa.

Brooks discloses exponent normalizing circuitry (Brooks, Fig. 6:630, normalizer

circuit) for bit-shifting the mantissa until the exponent is identical (Brooks, Colum 4,

lines 40-43 explains that normalization of the present invention requires shifting the

most significant binary "1" of the intermediate fraction or mantissa into the carry bit)

At the time of the invention, it would have been obvious to one ordinary skill in

the art to modify Toshihiko teachings by implementing the normalizer circuit to the

demodulator, as taught by Brooks.

The motivation would be to provide a demodulator which simplified the

completion of floating point arithmetic operations o two per-normalized operands by

performing in parallel the steps of normalizing and rounding the arithmetic result.

(Brooks, Colum 1, lines 15-18)


As per claim 3, Toshihiko in view of Brooks further discloses a device according

to either one of claims 1 or 2 wherein the predetermined minimum value Amin is zero

(Toshihiko, Fig. 2A, low rectify level, which is in this case minimum amplitude, page 10,

lines 10-13, explains that each level is prescribed), and the multi-stage binary search

circuitry (Toshihiko, Fig. 1,34:42, 1$^{st}$ and 2$^{nd}$ detector, which perform multi-stage binary

search) includes a first stage search element (Toshihiko, Fig. 1,34:42, 1$^{st}$ detector) and

one or more subsequent stage search elements (Toshihiko, Fig. 1, which sows

subsequent search elements), the first stage search element (Toshihiko, Fig. 1,34:42,

1$^{st}$ detector) including a bit shift block for determining the mid-point (Toshihiko, page 7,

lines 24-27) between the predetermined maximum value Amax (Toshihiko, Fig. 2A, high

rectify level, which is in this case maximum amplitude) and zero (Toshihiko, Fig. 2A, low

rectify level, which is in this case minimum amplitude, page 10, lines 10-13, explains

that each level is prescribed).

As per claim 4, Toshihiko in view of Brooks further discloses a device according

to claim 3, wherein each subsequent stage search elements (Toshihiko, Fig. 1, which

shows subsequent search elements) includes an adder (Toshihiko, Fig. 1:60, adder) for

determining the mid-point between upper and lower output values of a preceding search

element (Toshihiko, Fig. 2B, which shows the mid-point of HL and ML).

4.      Claims 5, and 11, are rejected under 35 U.S.C. 103(a) as being unpatentable

over Toshihiko and further in view of Brooks (US patent# 6185593 B1) and further in

view of Luo (US PGPUB# 2004/0095998 A1).

As per claim 5, Toshihiko in view of Brooks further discloses a device according

to claim 3, wherein the first stage search element (Toshihiko, Fig. 1,34:42, 1$^{st}$ detector)

and subsequent stage search elements (Toshihiko, Fig. 1, which shows subsequent

search elements) respectively the midpoint between predetermined maximum and

minimum values Amax (Toshihiko, Fig. 2A, high rectify level, which is in this case

maximum amplitude) and Amin (Toshihiko, Fig. 2A, low rectify level, which is in this

case minimum amplitude), and the midpoint between upper and lower output values of

a preceding search element (Toshihiko, Fig. 2B, which shows the mid-point of HL and

ML), and wherein the integer value k (Toshihiko, page 3, lines 11-21) is constructed by

the integer value constructing circuitry (Toshihiko, Fig. 1).

Toshihiko in view of Brooks does not disclose each include a comparator for

comparing.

Luo discloses each include a comparator for comparing (Fig. 1a and 1b,

122,123,124).

At the time of the invention it would have been obvious to one ordinary skill in the

art to modify Toshihiko in view of Brooks teachings by implementing the comparator to

the demodulator, as taught by Luo.

The motivation would be to provide a system which relates to motion estimation

for video encoding and more specifically to motion estimation based on a pyramid

structure with all binary representation for video encoding, as taught by Luo.

As per claim 11, Toshihiko in view of Brooks further discloses a device according

to claim 4, wherein the first stage search element (Toshihiko, Fig. 1,34:42, 1$^{st}$ detector)

and subsequent stage search elements (Toshihiko, Fig. 1, which shows subsequent

search elements) each include a comparator for comparing respectively the midpoint

between predetermined maximum and minimum values Amax (Toshihiko, Fig. 2A, high

rectify level, which is in this case maximum amplitude) and Amin (Toshihiko, Fig. 2A,

low rectify level, which is in this case minimum amplitude), and the midpoint between

upper and lower output values of a preceding search element (Toshihiko, Fig. 1, which

shows subsequent search elements), and wherein the integer value k (Toshihiko, page

3, lines 11-21) is constructed by the integer value constructing circuitry (Toshihiko, Fig.

1).

Toshihiko in view of Brooks does not disclose from the output of comparator.

Luo discloses from the output of comparator (Fig. 1a and 1b, 122,123,124).

At the time of the invention it would have been obvious to one ordinary skill in the

art to modify Toshihiko in view of Brooks's teachings by implementing the comparator to

the demodulator, as taught by Luo.

The motivation would be to provide a system which relates to motion estimation

for video encoding and more specifically to motion estimation based on a pyramid

structure with all binary representation for video encoding, as taught by Luo.


## Conclusion

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to SYED HAIDER whose telephone number is (571)270-

5169. The examiner can normally be reached on Monday thru Friday 8:00AM to 5:00

PM Est.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hai Tran can be reached on 571-272-5703. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.


/SH/

/GEORGE BUGG/
Primary Examiner, Art Unit 4147